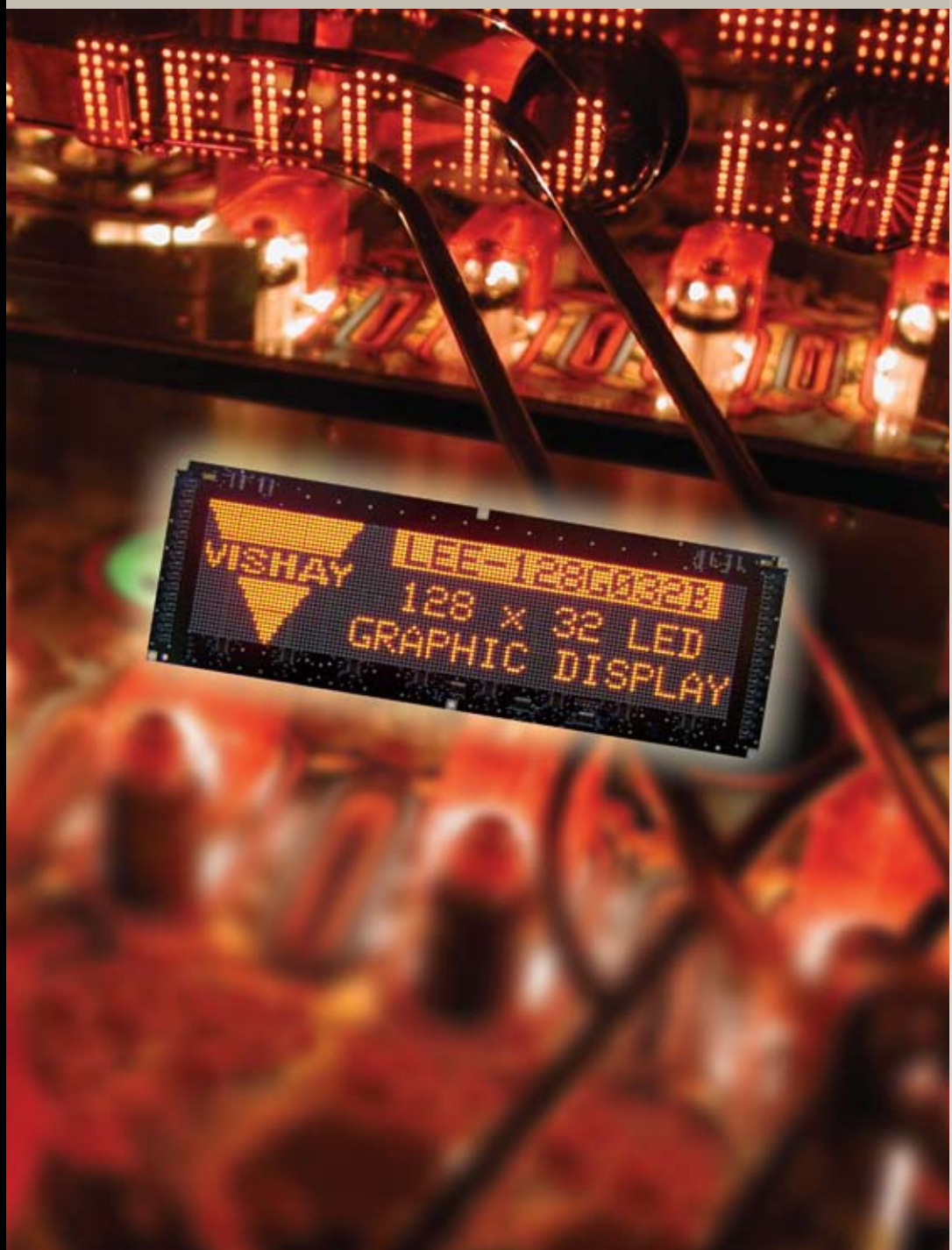
VISHAY INTERTECHNOLOGY, INC.

DISPLAYS

LED DISPLAY MODULES

LEE-128G032B

PRODUCT OVERVIEW



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LED DISPLAY MODULES

LEE-128G032B

128 x 32 Graphics Display with Drive Electronics and + 5 V HC CMOS Level Video Interface

The LEE-128G032B is an LED replacement for the popular APD-128G032 plasma display module. It is designed to offer high brightness and superior viewing characteristics in a slim package. This display is ideal for low to medium level information content and applications such as arcade games, process control, POS terminals, medical equipment, message centers and ATM machines.

The LEE-128G032B LED display offers high contrast, wide viewing angle, and long distance readability. It emits a bright red color which catches the attention of the viewer but is comfortable to the eye.

The LEE-128G032B LED display has a video type interface and is driven in a standard row/column refresh method. Pixel data is clocked for a row, and rows are scanned sequentially. Signals are presented for SERIAL DATA, DOT CLOCK, COLUMN LATCH, ROW DATA, ROW CLOCK and DISPLAY ENABLE. The SERIAL DATA is entered with the DOT CLOCK up to frequencies as high as 8 MHz. After a row of 128 pixels is clocked in, the COLUMN LATCH signal is toggled and the data is latched. At the time the data is latched, the display is briefly disabled using the DISPLAY ENABLE signal, then the row pointer is advanced with the ROW CLOCK signal. Once each frame the ROW DATA must be asserted to synchronize the column serial data with the beginning row. The recommended scanning frequency is approximately 70 Hz, but may be as high as 200 Hz.

Features

- LED replacement for the popular APD-128G032 plasma display module
- + 5 V HC CMOS level video interface
- Large characters
- Highly visible for long distance viewing
- > 30:1 contrast ratio
- Bright red color
- Slim profile
- Reduced power and brightness version

Pb-free
RoHS COMPLIANT

Electrical Specifications

Voltage(s) Required: + 5 V_{DC} (V_{CC})

Power Required (Fully Lit): Typical = 5.5 W
Maximum = 6.5 W

Optical Specifications

Viewing Area: 12.75" [323.8 mm] W x 3.15" [80.01 mm] L

Character Size (5 x 7): 0.65" [16.51 mm] H x
0.45" [11.43 mm] W

Pixel Size: 0.063" [1.6 mm] H x 0.031" [0.8 mm] W

Pixel Pitch: 0.100" [2.54 mm]

Luminance: 100 foot-lamberts minimum

Color: Bright red

Viewing Angle: > 150°

Environmental Specifications

Operating Temperature: - 40 °C to + 85 °C

Storage Temperature: - 40 °C to + 85 °C

Relative Operating Humidity: To 95 % non-condensing

Mechanical Shock: 30 G

Vibration: 3 G

Operating Altitude: 10 000 ft

Interface Signal Description

DOT CLOCK - This signal enters the SERIAL DATA on each low to high transition. A total of 128 DOT CLOCK transitions must be present for each line of column/anode data.

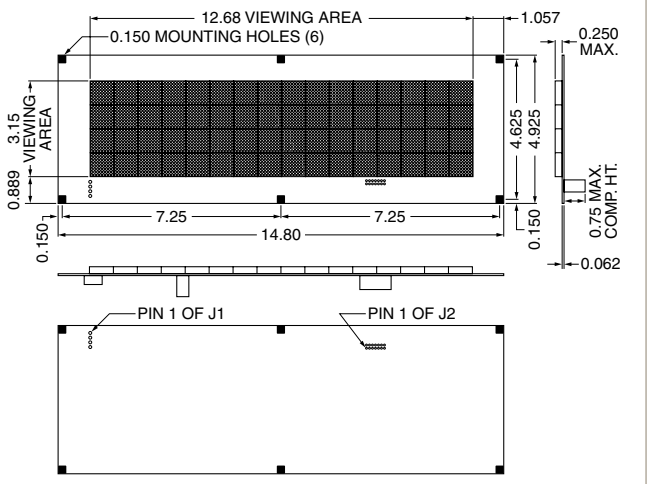
SERIAL DATA - This signal presents the pixel data in positive logic format. A logic one represents a lit pixel and a logic zero

Standard Electrical Specifications*

Description	Symbol	Min.	Typ.	Max	Units
Logic and LED Drive Voltage	V_{CC}	+ 4.5	+ 5.0	+ 5.5	V_{DC}
Logic and LED Drive Current (Fully Lit)	I_{CC}	–	1.1	1.3	A_{DC}
Logic 1 Input	V_{ih}	0.7 V_{CC}	–	–	V_{DC}
Logic 0 Input	V_{il}	–	–	0.3 V_{CC}	V_{DC}

*Recommended operating voltages. All maximums are absolute maximum.

Dimensions in inches



represents an extinguished pixel. Data is entered from right to left. The first pixel data entered will represent the left most pixel in the row.

COLUMN LATCH - This signal latches the pixel data into the driver outputs. When the COLUMN LATCH signal goes to logic one, the data entered previously will fall through to the driver outputs. When the signal returns to a logic zero, the data is latched, and the shift register is now ready to accept the next row of data. Must be held low while entering new SERIAL DATA.

DISPLAY ENABLE - This signal enables the output drivers. Using a duty cycle control, this signal may also be used for intensity control. The DISPLAY ENABLE must be at logic zero before the COLUMN LATCH signal transitions. To avoid display blurring, the ROW CLOCK signal should also transition while DISPLAY ENABLE is a logic zero.

ROW DATA - This signal is the first line marker for the scan. This input should be held high to correspond to the first row of pixel data.

ROW CLOCK - This signal clocks ROW DATA on the falling edge. The ROW CLOCK signal is repetitive and must be present for proper scanning of the display module. The LEE-128G032B has an unique input protection circuit that assures the column drivers stay blanked on power up. The protection circuit unblanks the column drivers when the ROW CLOCK signal begins (i.e., the display begins scanning.)

Pin Description

J2 – Power Connector

Molex 26-48-1045 or equivalent.
Mates with Tyco AMP 3-640428-4 or Molex 09-50-3041 housing with 08-50-0106 socket crimp terminals or equivalent.

Pin	Signal	Description
1	V_{CC}	Logic and LED drive supply
2	V_{CC}	Logic and LED drive supply
3	GND	Ground
4	GND	Ground

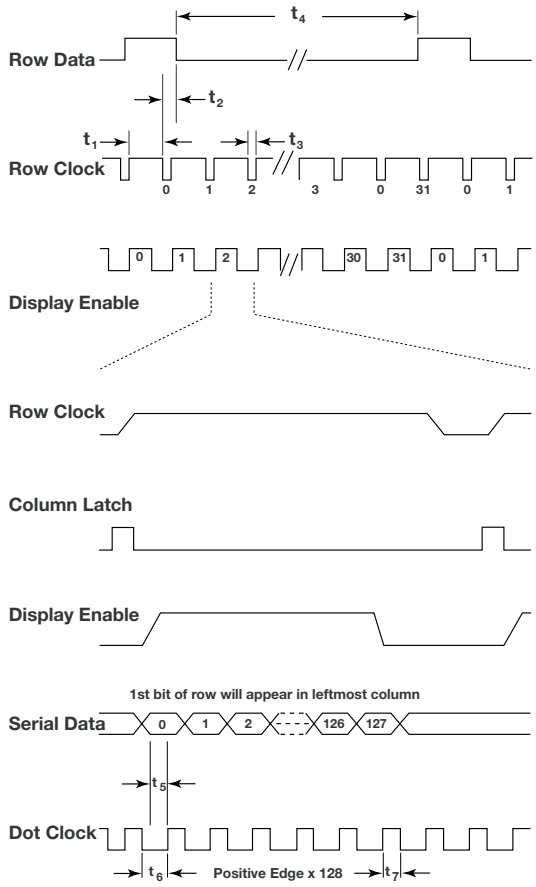
J1 – Data Connector

FCI 75869-102LF or equivalent.
Mates with Tyco AMP 1658621-2 or equivalent.

Pin	Description	Pin	Description
1	Display enable	2	Ground
2	Row data	4	Ground
5	Row clock	6	Ground
7	Column latch	8	Ground

*Recommended operating voltages. All maximums are absolute maximum.

Logic and Data Timing



Parameter	Min.	Typ.	Max.	Units
t_1	100	–	–	ns
t_2	5	–	–	µs
t_3	1	–	–	µs
t_4	–	70	200	Hz
t_5	25	–	–	ns
t_6	75	–	–	ns
t_7	75	–	–	ns

Ordering Information

Description	Part Number
Display, Driver Electronics and + 5 V HC CMOS Interface	LEE-128G032B
J1 Data Connector Kit (2 pcs. recommended)	280105-08
J2 Power Connector Kit	280108-16

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